Physical Layer and Media II

Digital-to-Digital Conversion 2/2

Agenda

Digital-to-Digital Conversion

- Line Coding Schemes – continue
    - Multilevel Schemes
    - Multitransition Schemes
- Redundancy
- Paired Disparity
- Block Coding
- Scrambling

Digital-to-Digital Conversion

Line Coding Schemes - Continue

In this section, we see how we can represent digital data by using digital signals.

The conversion involves three techniques: line coding, block coding, scrambling.

Line coding is always needed; block coding & scrambling may not be needed.

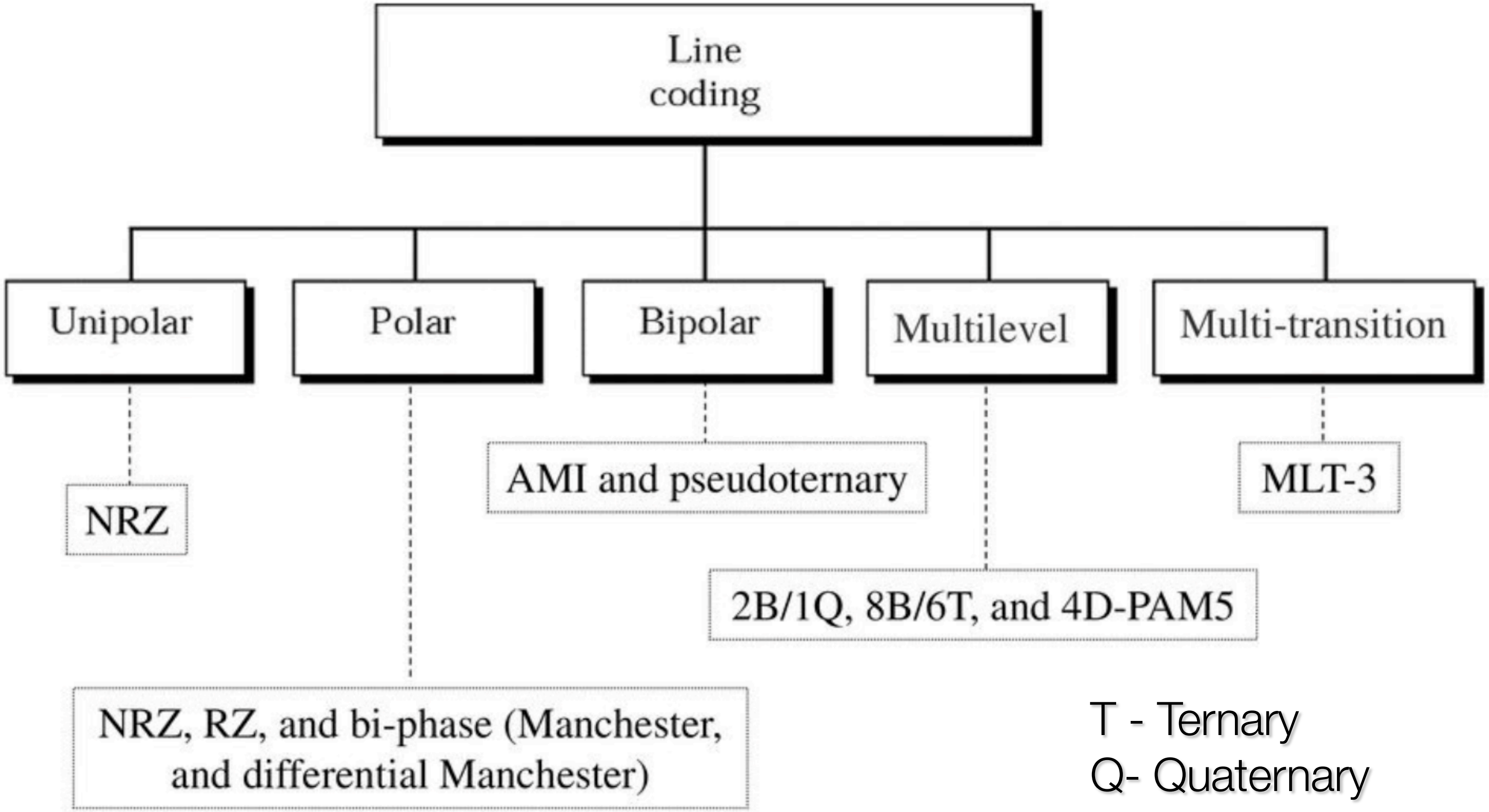
Digital Transmission Problems:
Synchronization, Bandwidth Size, DC component, Error detection/correction.

Solutions:

- Self-synchronization,
- Down a Rate bit/signal,
- Redundancy,
- Paired Disparity,
- Scrambling.

Digital-to-Digital Conversion

Line Coding Schemes Genealogy (Repeat)

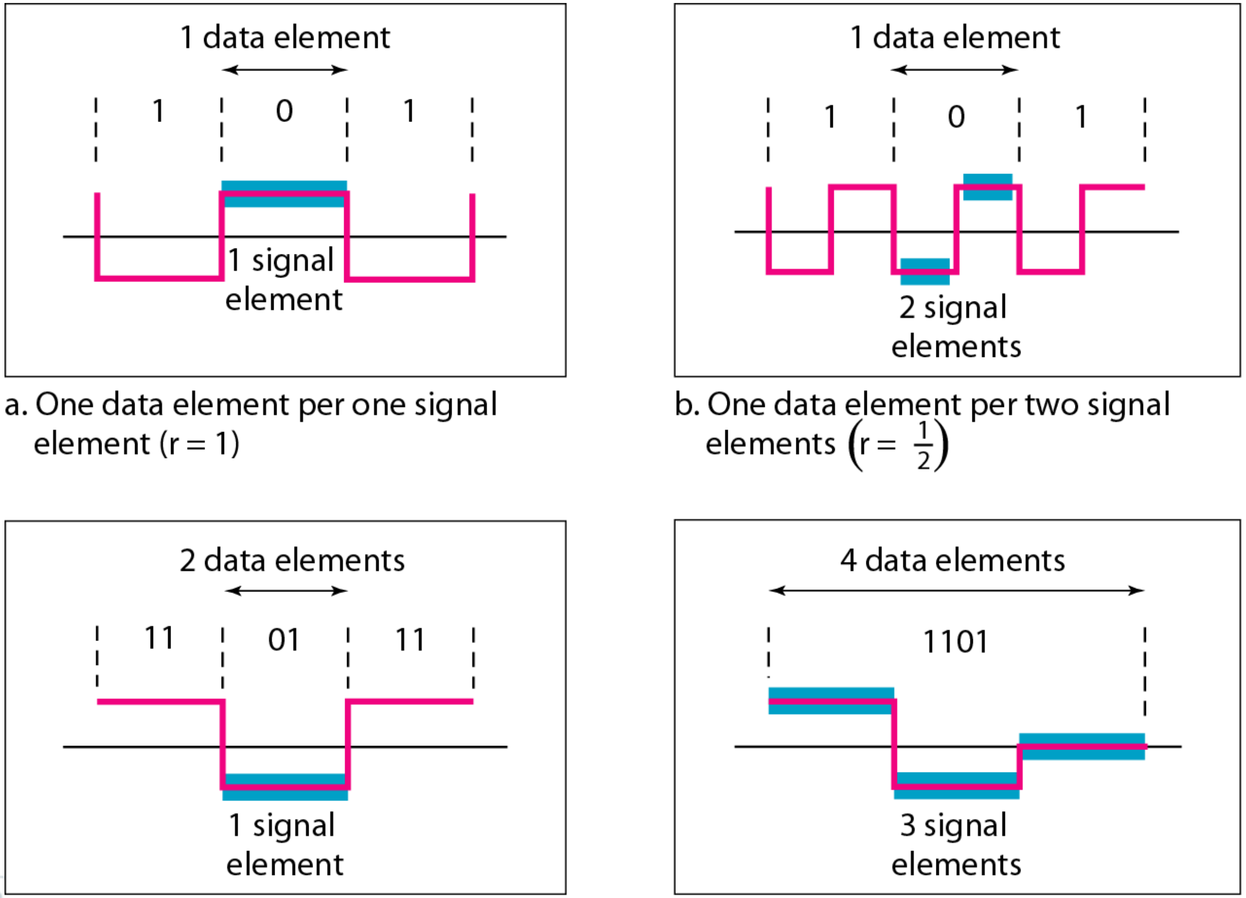


T - Ternary
Q- Quaternary

Digital-to-Digital Conversion

Signal Element and Data Element Range (Repeat)

Data elements are what we need to send; signal elements are what we can send



a. One data element per one signal element ($r = 1$)

b. One data element per two signal elements $\left(r = \frac{1}{2}\right)$

c. Two data elements per one signal element ($r = 2$)

d. Four data elements per three signal elements $\left(r = \frac{4}{3}\right)$

Digital-to-Digital Conversion

Implementation Different Codes to Fast and 100G Ethernet

Problem:

Baud-rate problem for bit-rate 100Mbps with Manchester code.
Manchester code **include a clock** signal with every data bit, bet it **doubles the baud-rate** of transmission (10Mbps data need 20Mbaud=20MHz).
Manchester code for 100Mbps need 200 MHz – its problem for transmit and over UTP-3 (certified only for 16MHz), and over UTP-5 (certified only for 100MHz).

Solution:

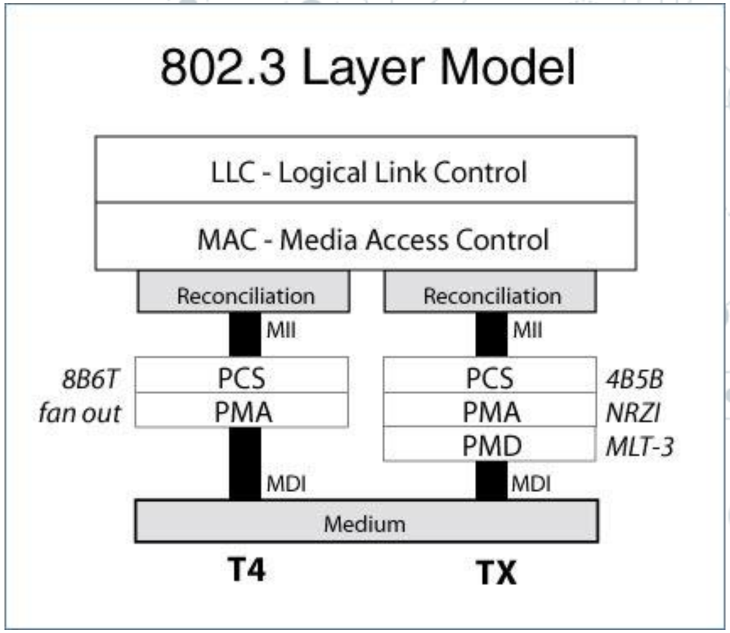
802.3 100BASE-TX/T4 standard uses combination of:

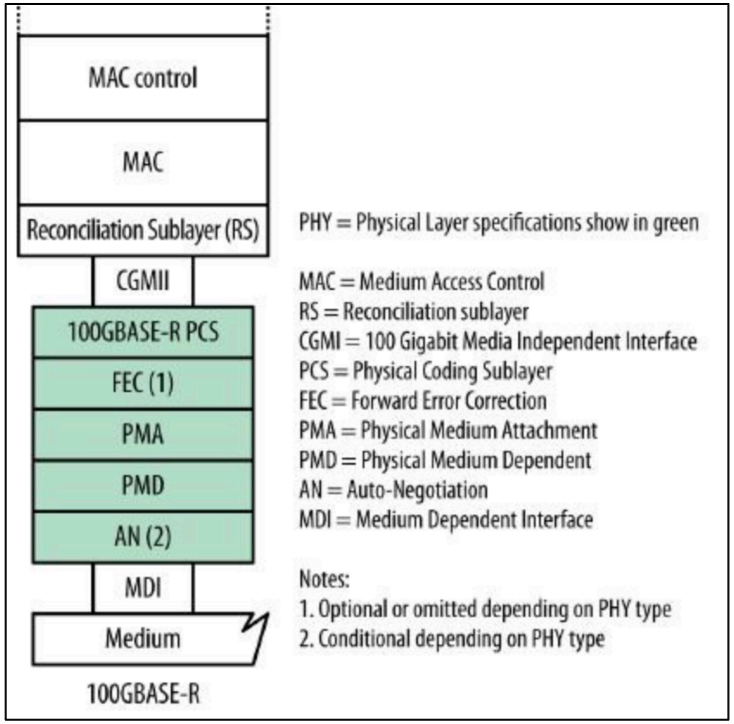
- 4B/5B (increase speed from 100Mbps to 125Mbps)
- NRZI (down frequency to 62,5MHz)
- MLT-3 (again down frequency to 31,25MHz)

or

- 8B6T (final slowdown frequency to 12,5MHz - transmit signal over to 3 cable pairs).

Wow !!! HOW??? Look on next slides!





Digital-to-Digital Conversion

Multilevel Schemes: Basic Theory

- In multilevel schemes we increase the number of data bits per symbol thereby increasing the bit rate.
- Since we are dealing with binary data we only have 2 types of data element a 1 or a 0.
- We can combine the 2 data elements into a pattern of “m” elements to create “2^m” symbols.
- If we have L signal levels, we can use “n” signal elements to create L^n signal elements.

- Now we have 2^m symbols and L^n signals.
- If $2^m > L^n$ then we cannot represent the data elements, we don’t have enough signals.
- If $2^m = L^n$ then we have an exact mapping of one symbol on one signal (simple dig2dig encoding schemes).
- If $2^m < L^n$ then we have more signals than symbols and we can choose the signals that are more distinct to represent the symbols and therefore have better noise immunity and error detection as some signals are not valid.

Digital-to-Digital Conversion

Multilevel Schemes: Representing Multilevel Codes, 2B1Q

Note

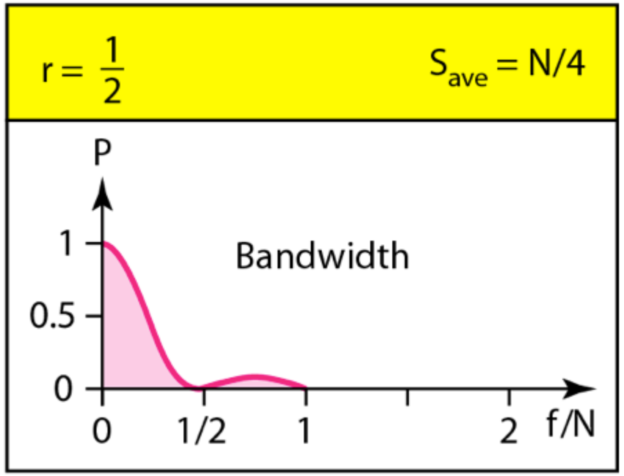
- In mBnL schemes, a pattern of m data elements is encoded as a pattern of n signal elements level in which $2^m \leq L^n$.

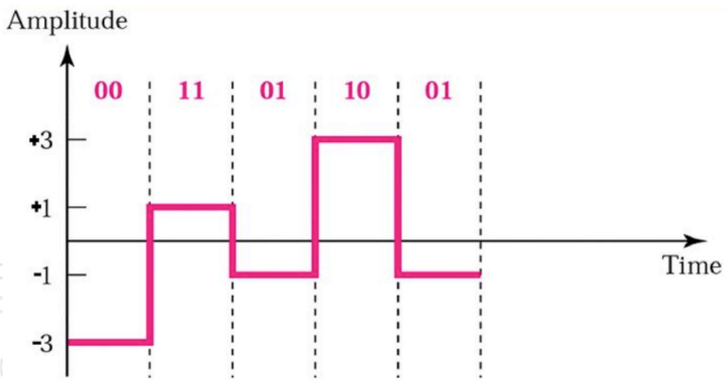
- We use the notation mBnL, where m is the length of the binary pattern, B represents binary data, n represents the length of the signal pattern and L the number of levels.

- L =B binary, L =T for 3 ternary, L =Q for 4 quaternary.

- Examples: 4B3T, 8B6T, 2B1Q.

- 2B1Q (used on ISDN and HDSL)





00	-3
01	-1
10	+3
11	+1

Digital-to-Digital Conversion

Multilevel Schemes: Redundancy and Paired Disparity

- In the 2B1Q scheme we have **no redundancy ($B^2=2^2=4$ ~ $Q^1=4^1=4$)** and we see that a **DC component is present**.

- If we use a code with redundancy we can decide to use only "0" or "+" weighted codes (more +'s than -'s in the signal element) and invert any code that would create a DC component. E.g. '+00++-' -> '-00--+'

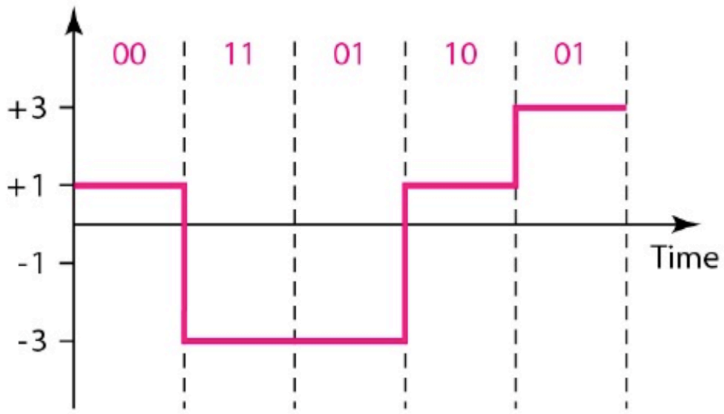
- This technique is called Paired Disparity.

- Paired disparity code is a line code in which at least one of the data characters is represented by two codewords of opposite disparity that are used in sequence so as to minimize the total disparity of a longer sequence of digits.
- The simplest paired disparity code is AMI (Alternate Mark Inversion signal.
- Other paired disparity codes include 8B/10B, 8B/12B, modified AMI, 4B3T, modify 2B1Q.

Digital-to-Digital Conversion

Multilevel Schemes: modify 2B1Q with Paired Disparity

- In the modify 2B1Q scheme uses Paired Disparity Codes, so we do have **DC component is no present.**



Assuming positive original level

	Previous level: positive	Previous level: negative
Next bits	Next level	Next level
00	+1	-1
01	+3	-3
10	-1	+1
11	-3	+3

Transition table

Digital-to-Digital Conversion

Multilevel Schemes: 4B3T (Ex. of Paired Disparity Code)

4 Bit → 3 Signal

- 4B3T used on Prior ISDN Interface
- We have $2^4 = 16$ input combinations to represent, $3^3 = 27$ output combinations.
- 000 is not used to avoid long periods without a transition.
- 4B3T uses a Paired Disparity Code to achieve an overall zero DC component: When transmitting, the DC component is tracked and a combination chosen that has a DC component of the opposite sign to the running total.
- Encoding table - This code forces a transition after at most five consecutive identical non-zero symbols, or four consecutive zero symbols.
- Decoding table - Decoding is simpler, as the decoder does not need to keep track of the encoder state.

Digital-to-Digital Conversion

Multilevel Schemes: 4B3T (Encoding-Decoding Tables)

<table>
<tr><th colspan="2">Input</th><th colspan="4">Accumulated DC offset</th></tr>
<tr><th>Hex</th><th>Binary</th><th>1</th><th>2</th><th>3</th><th>4</th></tr>
<tr><td>0</td><td>0000</td><td>+ 0 + (+2)</td><td colspan="3">0–0 (–1)</td></tr>
<tr><td>1</td><td>0001</td><td colspan="4">0 – + (+0)</td></tr>
<tr><td>2</td><td>0010</td><td colspan="4">+ – 0 (+0)</td></tr>
<tr><td>3</td><td>0011</td><td colspan="3">0 0 + (+1)</td><td>– – 0 (–2)</td></tr>
<tr><td>4</td><td>0100</td><td colspan="4">– + 0 (+0)</td></tr>
<tr><td>5</td><td>0101</td><td>0 + + (+2)</td><td colspan="3">– 0 0 (–1)</td></tr>
<tr><td>6</td><td>0110</td><td colspan="2">– + + (+1)</td><td colspan="2">– – + (–1)</td></tr>
<tr><td>7</td><td>0111</td><td colspan="4">– 0 + (+0)</td></tr>
<tr><td>8</td><td>1000</td><td colspan="3">+ 0 0 (+1)</td><td>0 – – (–2)</td></tr>
<tr><td>9</td><td>1001</td><td colspan="3">+ – + (+1)</td><td>– – – (–3)</td></tr>
<tr><td>A</td><td>1010</td><td colspan="2">+ + – (+1)</td><td colspan="2">+ – – (–1)</td></tr>
<tr><td>B</td><td>1011</td><td colspan="4">+ 0 – (+0)</td></tr>
<tr><td>C</td><td>1100</td><td>+ + + (+3)</td><td colspan="3">– + – (–1)</td></tr>
<tr><td>D</td><td>1101</td><td colspan="3">0 + 0 (+1)</td><td>– 0 – (–2)</td></tr>
<tr><td>E</td><td>1110</td><td colspan="4">0 + – (+0)</td></tr>
<tr><td>F</td><td>1111</td><td>+ + 0 (+2)</td><td colspan="3">0 0 – (–1)</td></tr>
</table>

Ternary	Binary	Hex
0 0 0	N/A	N/A
+ 0 +	0000	0
0 – 0	0000	0
0 – +	0001	1
+ – 0	0010	2
0 0 +	0011	3
– – 0	0011	3
– + 0	0100	4
0 + +	0101	5
– 0 0	0101	5
– + +	0110	6
– – +	0110	6
– 0 +	0111	7
+ 0 0	1000	8
0 – –	1000	8
+ – +	1001	9
– – –	1001	9
+ + –	1010	A

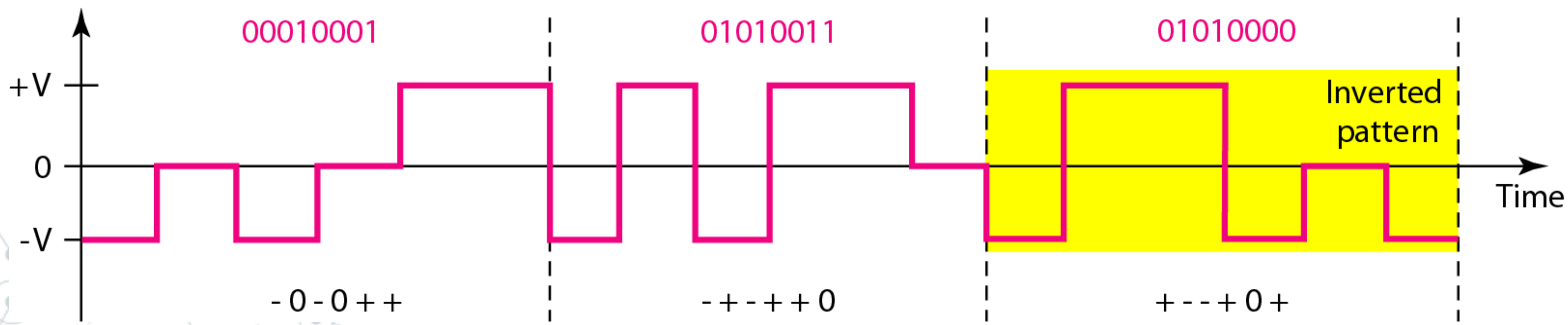
Ternary	Binary	Hex
+ – –	1010	A
+ 0 –	1011	B
+ + +	1100	C
– + –	1100	C
0 + 0	1101	D
– 0 –	1101	D
0 + –	1110	E
+ + 0	1111	F
0 0 –	1111	F

Digital-to-Digital Conversion

Multilevel Schemes: 8B6T (Ex. Paired Disparity Code)

8 Bit → 6 Signal

- The idea is to encode a pattern of 8 bits as a pattern of 6 signal elements, where the signal has three levels (ternary).
- In this type of scheme, we can have 2^8=256 different data patterns and 3^6=478 different signal patterns.
- There are 478-256=222 redundant signal elements that provide synchronization, DC component remove and error detection.
- Used on Fast Ethernet
- The average signal rate of the scheme is theoretically Save=1/2*N*6/8
- The minimum bandwidth equal 6N/8



Digital-to-Digital Conversion

Multilevel Schemes: Using multiple channels

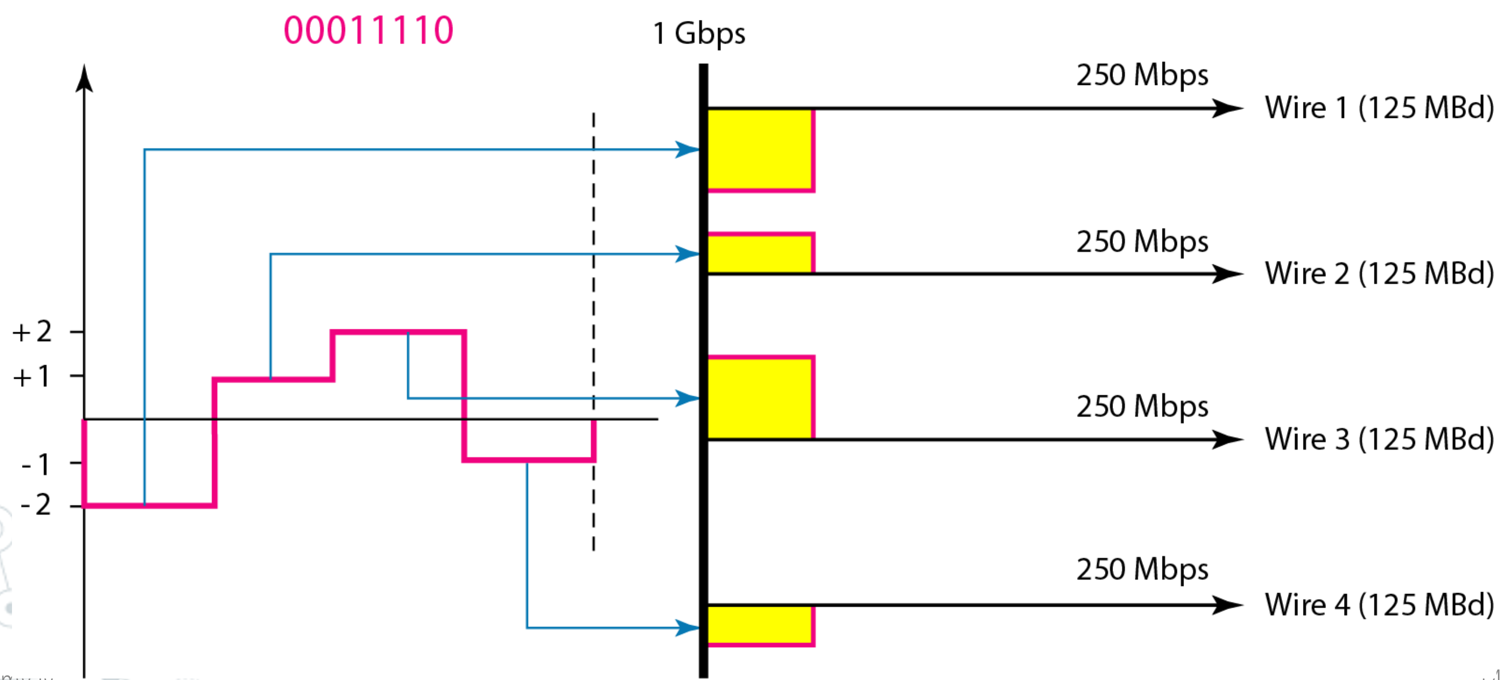
- In some cases, we split the signal transmission up and distribute it over several links.
- The separate segments are transmitted simultaneously. This reduces the signalling rate per link -> lower bandwidth.
- This requires all bits for a code to be stored.
- xD: means that we use ‘x’ links
- YYYz: We use ‘z’ levels of modulation where YYY represents the type of modulation (e.g. pulse ampl. mod. PAM).
- Codes are represented as: xD-YYYz

Digital-to-Digital Conversion

Multilevel Schemes: 4D-PAM5

4D-PAM5 - four dimensional pulse amplitude modulation five-level.

- The 4D means that data is sent over four wires at the **same time**.
- It uses five voltage levels, such as -2, -1, 0, 1, and 2.
- Level 0, is used only for forward error detection.
- If we assume that the code is just one-dimensional, the four levels create something similar to 8B4Q.
- All 8 bits can be fed into a wire simultaneously and sent by using one signal element.
- Used 1000BASE-T.
- Wow !!!



Digital-to-Digital Conversion

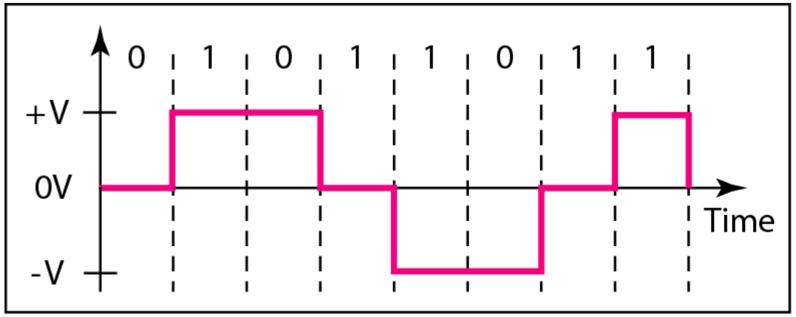
Multitransition Coding Schemes

Basic Theory

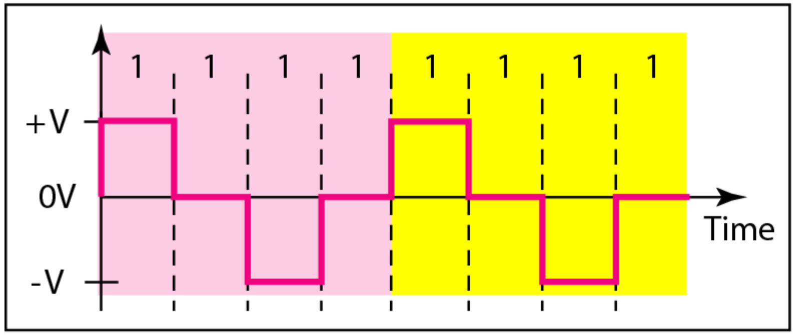
- Because of synchronization requirements we force transitions. This can result in very high bandwidth requirements -> more transitions than are bits (e.g. mid bit transition with inversion).
- Codes can be created that are differential at the bit level forcing transitions at bit boundaries. This results in a bandwidth requirement that is equivalent to the bit rate.
- In some instances, the bandwidth requirement may even be lower, due to repetitive patterns resulting in a periodic signal.

Digital-to-Digital Conversion

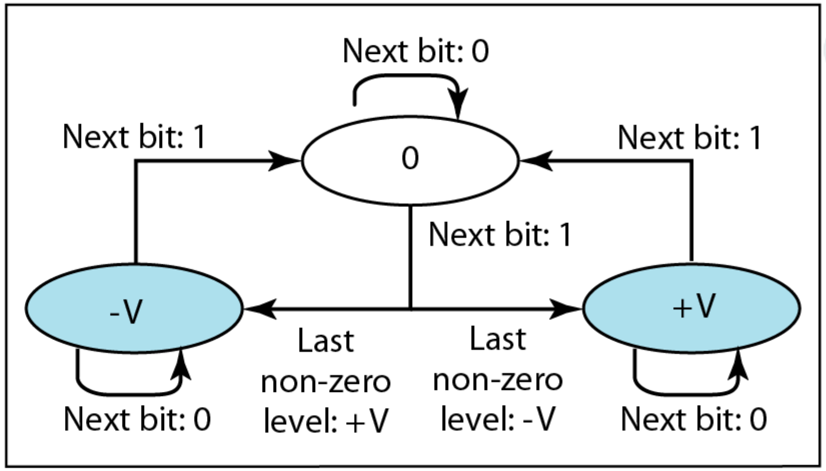
Multitransition Schemes: MLT-3



a. Typical case



b. Worse case



c. Transition states

- Signal rate is same as NRZ-I
- But because of the resulting bit pattern, we have a periodic signal for worst case bit pattern: 1111
- This can be approximated as an analog signal a frequency 1/4 the bit rate!

Digital-to-Digital Conversion

Line Coding Schemes Summary

Category	*Scheme*	*Bandwidth (average)*	*Characteristics*
Unipolar	NRZ	$B = N/2$	Costly, no self-synchronization if long 0s or 1s, DC
Polar	NRZ-L	$B = N/2$	No self-synchronization if long 0s or 1s, DC
	NRZ-I	$B = N/2$	No self-synchronization for long 0s, DC
	Biphase	$B = N$	Self-synchronization, no DC, high bandwidth
Bipolar	AMI	$B = N/2$	No self-synchronization for long 0s, DC
Multilevel	2B1Q	$B = N/4$	No self-synchronization for long same double bits
	8B6T	$B = 3N/4$	Self-synchronization, no DC
	4D-PAM5	$B = N/8$	Self-synchronization, no DC
Multitransition	MLT-3	$B = N/3$	No self-synchronization for long 0s

Digital-to-Digital Conversion

Line Coding Schemes Exercises

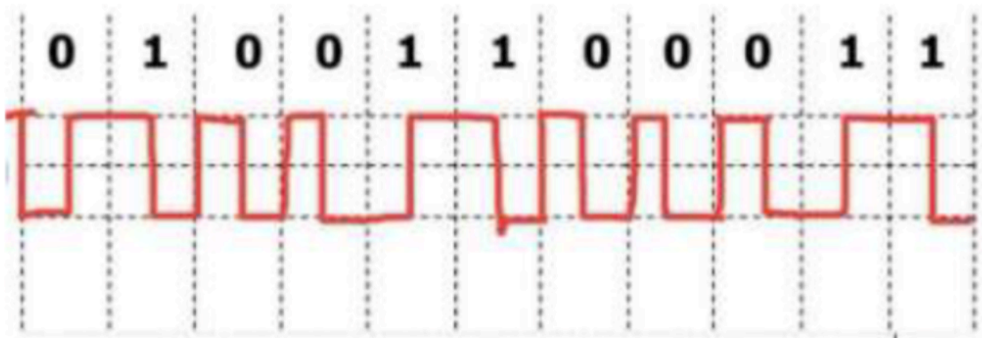
1. Draw the graph of the NRZ-L, NRZ-I, Manchester, Differential Manchester, MLT-3 schemes using each of the following data streams, assuming that the last signal level has been positive.

a) 00000000
b) 11111111
c) 01010101
d) 00110011
e) 00011000

2. Draw the graph of the 2B1Q scheme using each of the following data streams, assuming that the last signal level has been positive.

a) 00000000 00000000
b) 11111111 11111111
c) 01010101 01010101
d) 00110011 00110011

3. What is the encoding technique used in the Figure?



Digital-to-Digital Conversion

Block Coding Schemes

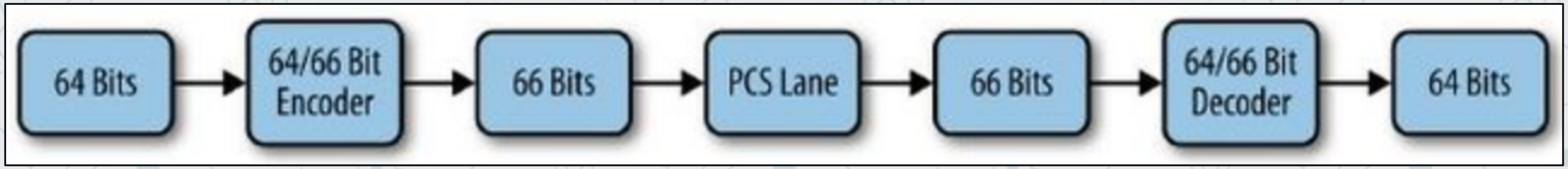
Basic Theory

- For a code to be capable of error detection, we need to add redundancy, i.e., extra bits to the data bits.

- Synchronization also requires redundancy - transitions are important in the signal flow and must occur frequently.
- Block coding is referred to as an mB/nB encoding technique. It is distinguished from multilevel coding by use of the slash - mB/nB.

- Block coding is done in three steps: Division, Substitution and Combination.

- The resulting bit stream prevents certain bit combinations that when used with line encoding would result in DC components or poor synchronization quality.
- Example, 64b/66b encoding scheme use on 10/40/100GB Ethernet



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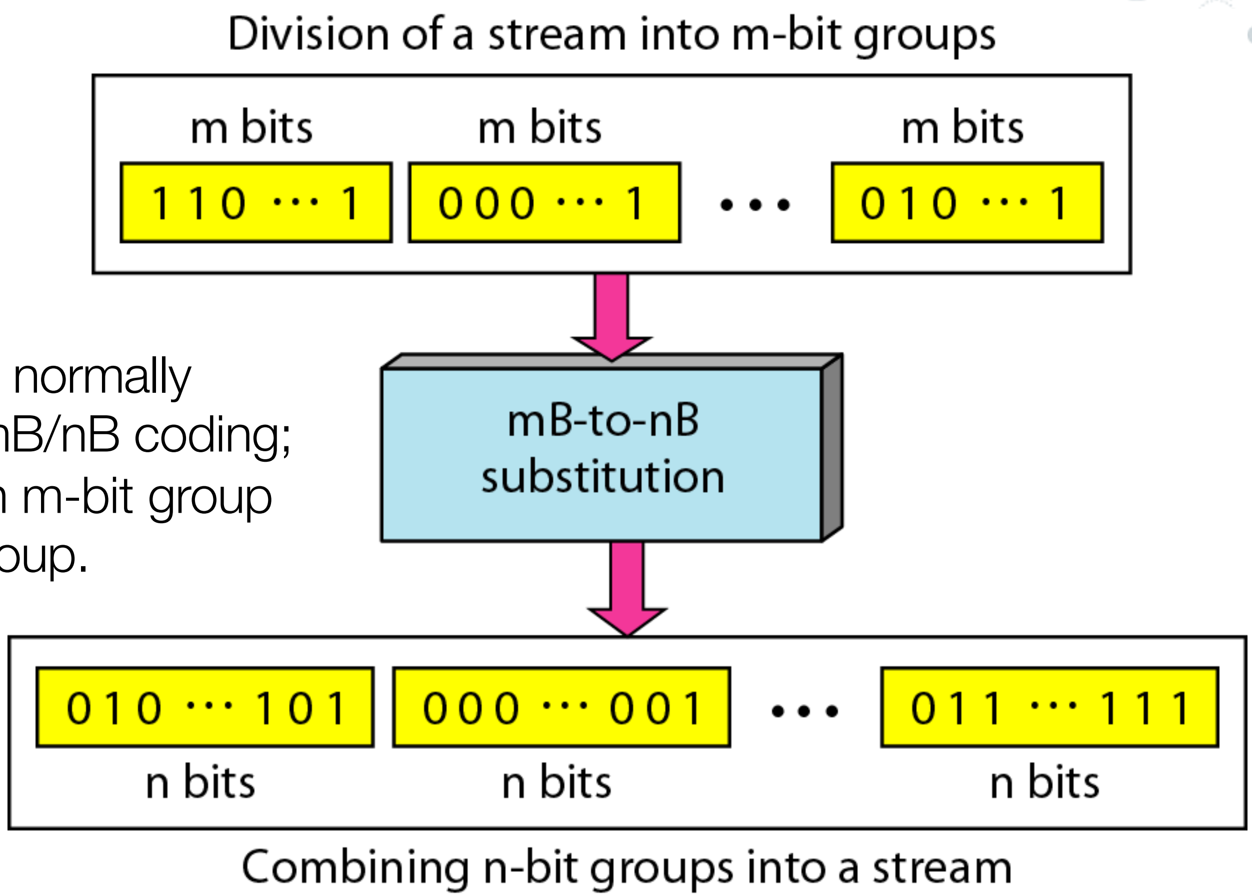
Block Coding: Concept



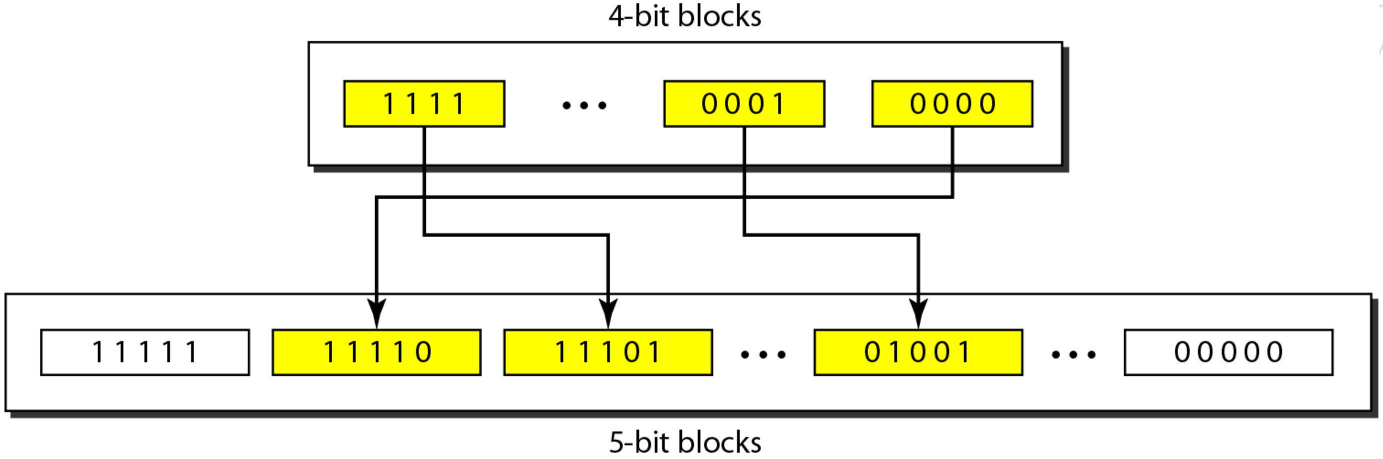
Note

- Block coding is normally referred to as mB/nB coding;
- it replaces each m-bit group with an n-bit group.

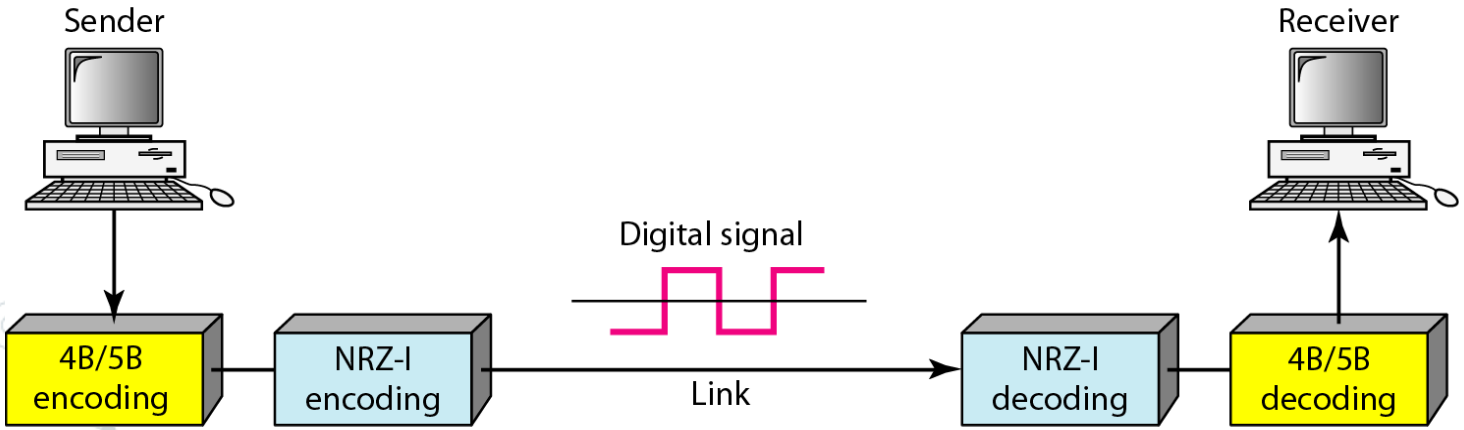
Digital-to-Digital Conversion

Block Coding: 4B/5B with NRZ-I

Substitution block coding 4B/5B.



Using block coding 4B/5B with NRZ-I line coding scheme.



Digital-to-Digital Conversion

Block Coding: 4B/5B Mapping table and Redundancy

Data Sequence	*Encoded Sequence*	*Control Sequence*	*Encoded Sequence*
0000	11110	Q (Quiet)	00000
0001	01001	I (Idle)	11111
0010	10100	H (Halt)	00100
0011	10101	J (Start delimiter)	11000
0100	01010	K (Start delimiter)	10001
0101	01011	T (End delimiter)	01101
0110	01110	S (Set)	11001
0111	01111	R (Reset)	00111
1000	10010		
1001	10011		
1010	10110		
1011	10111		
1100	11010		
1101	11011		
1110	11100		
1111	11101		

4B/5B Redundancy

A 4 bit data word can have 2^4=16 combinations.
A 5 bit word can have 2^5=32 combinations.
We therefore have 32 - 16 = 16 extra words.
Some of the extra words are used for control/signaling purposes.

Digital-to-Digital Conversion

Block Coding: 4B/5B vs Manchester (1B/2B)

Exercise. We need to send data at a 1-Mbps rate.
What is the minimum required bandwidth, using a combination of 4B/5B and NRZ-I or Manchester coding?

Solution

4B/5B block coding increases the bit rate to 1.25 Mbps.

The minimum bandwidth using NRZ-I is r=N/2 or 625 kHz.
The Manchester scheme r=1 needs a minimum bandwidth of 1.25 MHz.

The first choice needs a lower bandwidth, but has a DC component problem.
The second choice needs a higher bandwidth, but does not have a DC component problem.

Digital-to-Digital Conversion

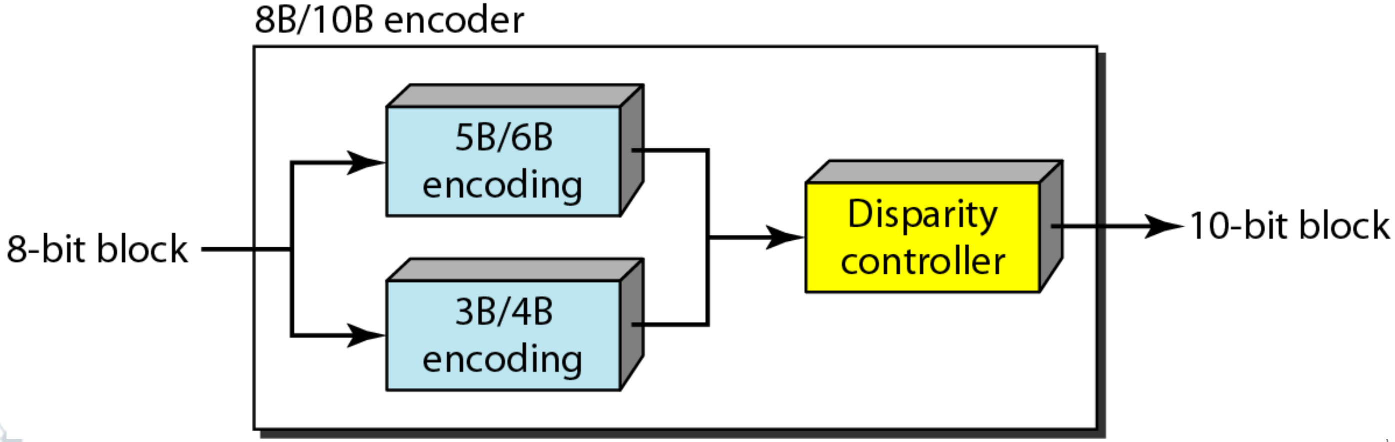
Block Coding: 8B/10B

More bits - better error detection.

- The 8B/10B block code adds more redundant bits and therefore has no problems with DC components, has no synchronization problems, and has error control.
- IBM realization (1983).
- 8B/10B used Fibre Chanel, Gigabit Ethernet, Display Port, PCI Expres and more.

3B4B Coding	
Input	Output
000	- - + - or + + - +
001	- - + +
010	- + - +
011	- + + -
100	+ - - +
101	+ - + -
110	+ + - -
111	- + - - or + - + +

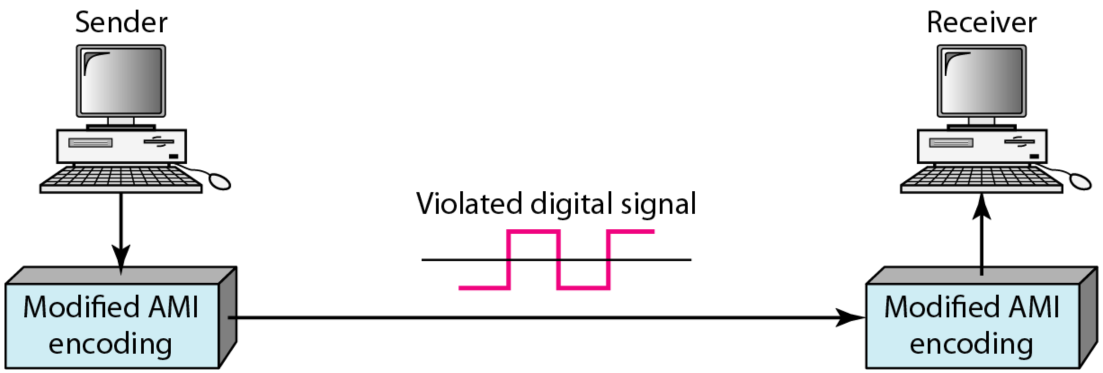
- Other example 64B/65B 10GBASE-T look https://en.wikipedia.org/wiki/Ethernet_over_twisted_pair



Digital-to-Digital Conversion

Scrambling: Concept

- The best code is one that does not increase the bandwidth for synchronization and has no DC components.
- Scrambling is a technique used to create a sequence of bits that has the required signal changes for transmission - self clocking, no low frequencies (no DC), no wide bandwidth.
- It is implemented at the same time as encoding, the bit stream is created on the fly.
- It replaces 'unfriendly' sequences of bits with a violation code that is easy to recognize.
- Modified AMI code used with HDB3 and 8BZS for Gigabit Ethernet.
- HDB3 – High Density Bipolar of order 3 code



Digital-to-Digital Conversion

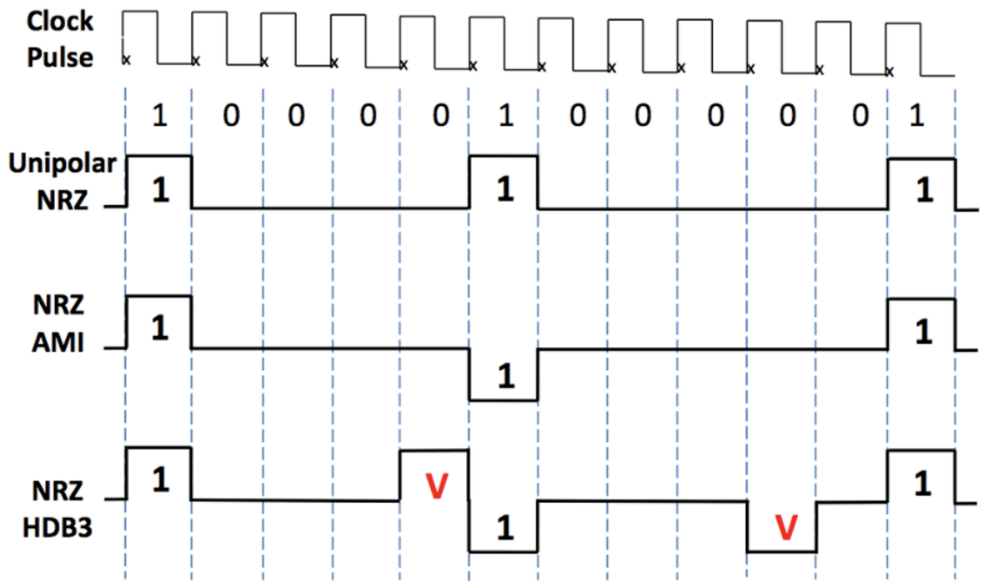
Scrambling: HDB3 (European for Multiplexing Carrier E-1,2,3)

HDB3 is a line code developed to avoid long strings of zeros in a data stream. It uses AMI (alternate mark inversion) coding. There are four rules for HDB3 coding:

(1) More than three consecutive zeros are not allowed to be present in the data waveform. For the fourth zero the code inserts a "violation bit" denoted by "**V**".
(2) Violation bits have to be of the same polarity as the previous mark.
(3) Two consecutive "violation bits" must be of opposite polarity.
(4) If the number of marks between two consecutive violation bits is even, the format must be **B**00**V**, where bit "**B**" is a stuffing bit and of opposite polarity to the previous mark. If the number of marks is an odd number, the format should be 000**V**.

HDB3 – High Density Bipolar of order 3 code

Parity of +/– bits since previous V	Pattern	Previous pulse	Coded
Even	B00V	+	–00–
		–	+00+
Odd	000V	+	000+
		–	000-

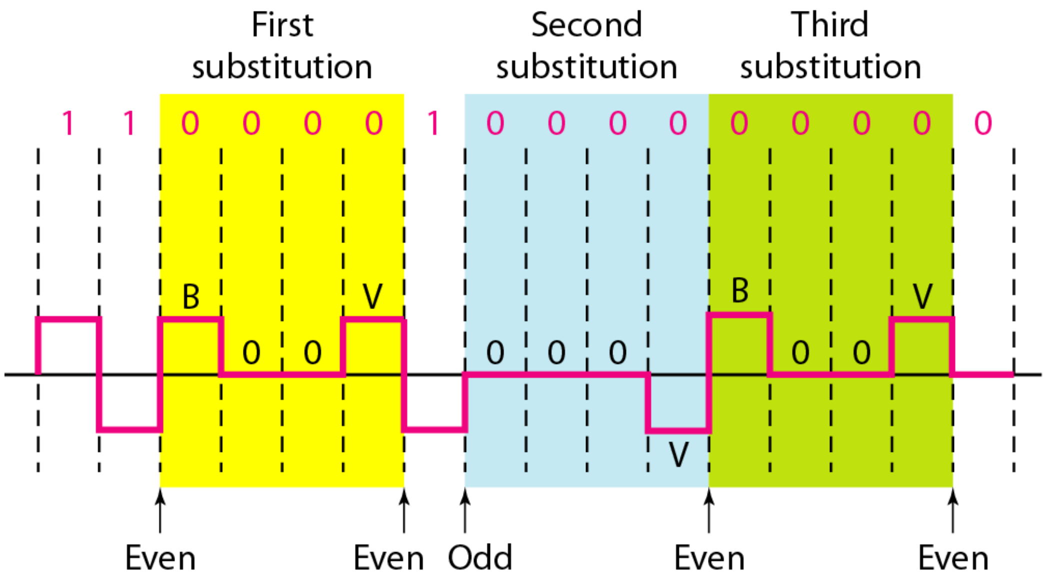


Digital-to-Digital Conversion

Scrambling: HDB3 (Cont. 1)

- HDB3 used in all levels of the European E-carrier system (E1,E2,E3)

Different situations in HDB3 scrambling technique



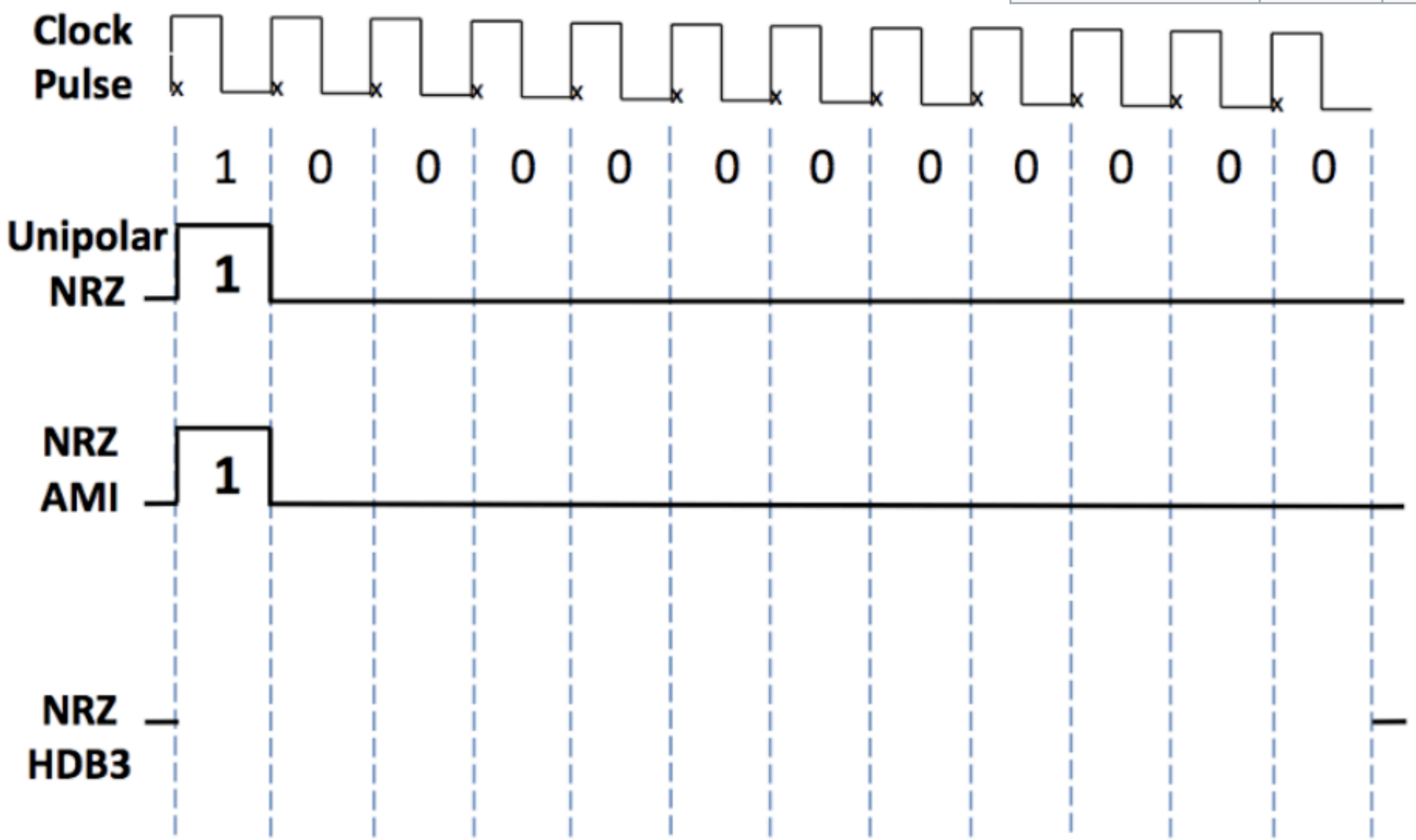
Parity of +/– bits since previous V	Pattern	Previous pulse	Coded
Even	B00V	+	–00–
		–	+00+
Odd	000V	+	000+
		–	000-

Digital-to-Digital Conversion

Scrambling: HDB3 - Exercise

Parity of +/– bits since previous V	Pattern	Previous pulse	Coded
Even	B00V	+	–00–
		–	+00+
Odd	000V	+	000+
		–	000-

Draw the correct HDB3 coding for this string of 12 bits.



Digital-to-Digital Conversion

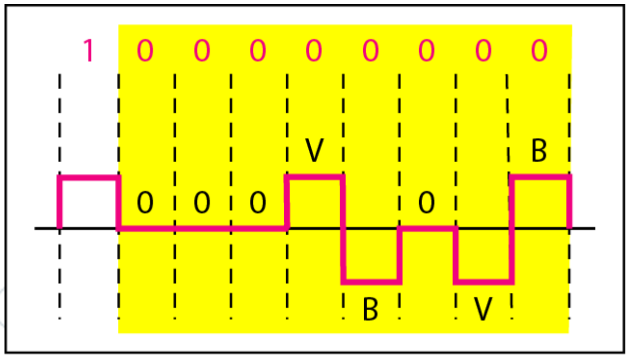
Scrambling: BXZS (American for Multiplexing Carrier T-1,2,3)

- B8ZS used in the North American T1 (1.544 Mbit/s) line code
- B6ZS used in the North American T2 (6.312 Mbit/s) line code
- B3ZS used in the North American T3 (44.736 Mbit/s) line code

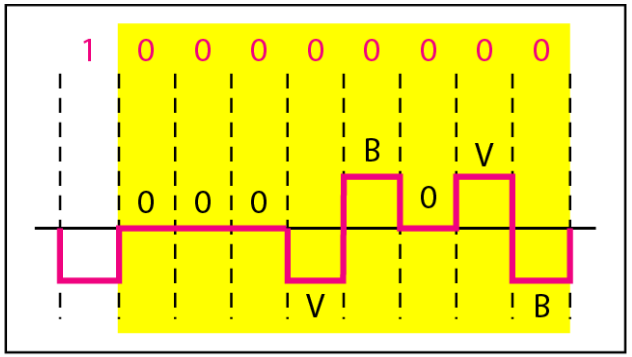
For example:

- B8ZS substitutes eight consecutive 0's with 000VB0VB.
- The V stands for violation, it violates the line encoding rule
- B stands for bipolar, it implements the bipolar line encoding rule

Two cases of B8ZS scrambling technique with disparity



a. Previous level is positive.



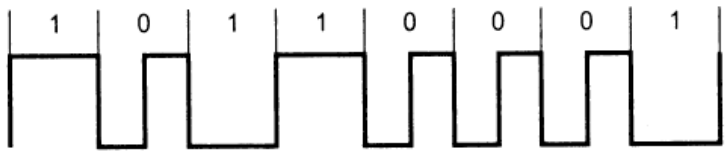
b. Previous level is negative.

Digital-to-Digital Conversion

Line Coding Schemes: Other Examples Line & Block Codes

FM0 (Frequency Modulation) uses on LocalTalk

- For 1 change on border of bit-interval +V to -V
- For 0 change inside bit interval



ASI (Alternative Space Inversion) or MAMI (Modified Alternate Mark Inversion) uses ISDN. Its inverted AMI

- For 0 change +V to –V to +V.. For 1 = 0V

HDB2 (High Density BiPolar 2)

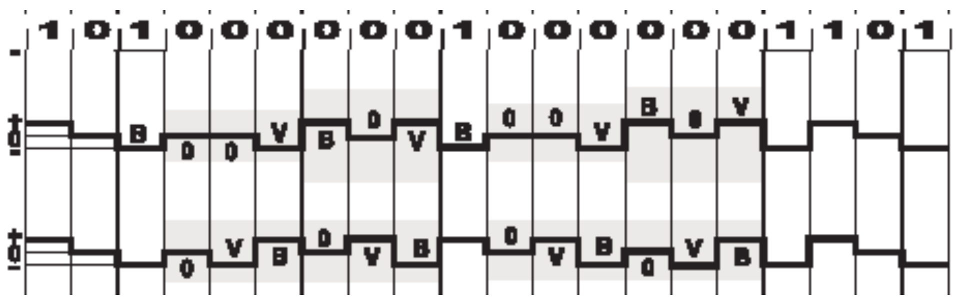
It like HDB3, bet for every 000 need change to 00V or B0V

B6ZS (Bipolar with 6 Zero Substitution)

It like B8ZS, bet for every 000000 need change to 0VB0VB

B3ZS (Bipolar with 3 Zero Substitution)

It like B8ZS, bet for every 000 need change to B0V or 00V



128B/130B, 128B/132B

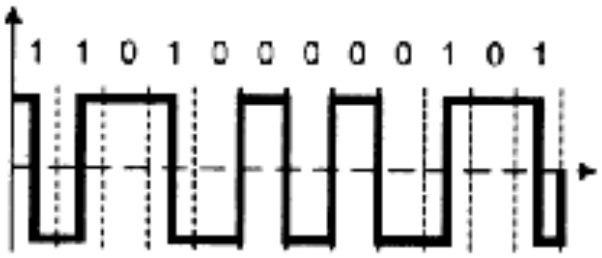
It like 8B10B and change this code for PCI Express 3 and for USB-3)

Digital-to-Digital Conversion

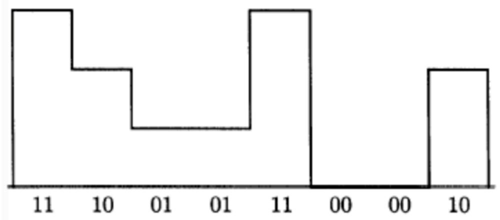
Line Coding Schemes: Other Examples Line & Block Codes

Millara Code

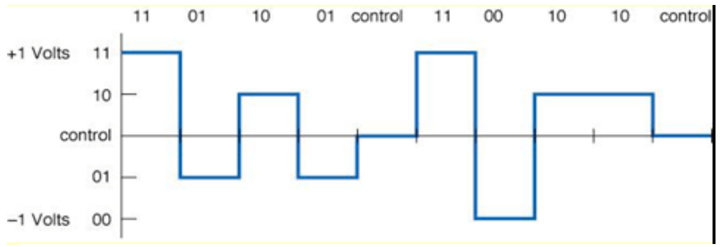
- 1 - signal changes in the middle of the interval
- 0 - signal after 1's does not change
- If two 0's repeat, then signal changes between them on start of interval.



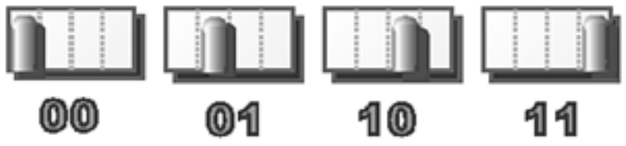
PAM4 (Pulse Amplitude Modulation 4) - unipolar



PAM5 (like PAM4) – bipolar, and 0's control symbol



PPM (Pulse Position Modulation) – signal in concrete position.



PWM (Pulse Width Modulation) – different pulse length.

PFM (Pulse Frequency Modulation) – concrete number of pulses in a period of time.